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A High Step-Up Interleaved DC-DC Converter With Voltage Multiplier and Coupled Inductors for Renewable Energy Systems

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ABSTRACT This paper proposes a new interleaved non-isolated high step-up dc-dc converter for interfacing renewable energy applications. The proposed converter achieves a very high step-up voltage gain by using two coupled inductors and a voltage multiplier cell. This topology utilizes the interleaved boost converter in the input side, and the input current is shared with low ripple. Moreover, a voltage multiplier cell with the secondary windings of the coupled inductors is employed in the output side to achieve the interleaved energy storage. The voltage stress on the semiconductor switches and the passive components is significantly reduced and lower than the output voltage. The aforementioned converter can be operated without an extreme duty cycle or a high turns ratio. The reverse recovery problem of the diodes is mitigated, and the leakage energy is recycled. Furthermore, by implementing low-voltage-rated MOSFETs with a small ON-resistance, the conduction losses can be reduced, and the efficiency can be improved. The topology is fed by a single input voltage, and the mathematical expression is methodically explored. The operation principle of the proposed converter and the comparison between the proposed converter with other topologies are discussed. The design, parameters selection, and experimental results are thoroughly introduced. A 32 to 800 V-dc is verified and simulated by using PLECS. Consequently, a 400 W hardware prototype is verified to validate the theory and the design.

INDEX TERMS Coupled inductors, high voltage gain, high step-up dc-dc converter, high efficiency, interleaved boost converter, PV, renewable energy systems, voltage multiplier.

I. INTRODUCTION

The demand for renewable energy systems, such as photovoltaic systems, fuel cells and wind turbines, has been robust in recent years. High step-up dc-dc converters are currently being utilized in many applications, such as dc distribution systems, data centers and telecom centers. Power electronic converters play a substantial role in power conversion of the distributed generation and the grid integration [1]. Increasing renewable energy sources would exceedingly catalyze the utilize of high step-up dc-dc power electronic converters to integrate renewable energy systems to electric power grid. Furthermore, power electronic converters should be highly efficient and reliable to convert the renewable energies to

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the electric power grid. As a result, using high step-up dc-dc converts with high efficiency is required, and it is the main goal to ensure the reliability. PV system technologies are still the most favorable technologies for a huge portion of renewable energy generation [2]. Nowadays, PV systems have the largest growth and installation between other renewable energy systems. Moreover, PV systems are receiving higher power ratings, and the grid side would request the PV inverter to steady the grid voltage. The grid connected PV systems have the advantage over the off-grid PV systems in terms of the growth and the installed PV systems. Since the output voltage of a PV panel is low (from 15 V to 50 V), a high dc-dc converter is compulsory to lift and regulate the output voltage of a PV panel to the voltage level of the DC-bus, which would be transferred to an AC voltage through an inverter to the load as shown in Fig. 1. Therefore, integrating a PV panel to a 800 V dc is perceptibly a rigid duty and entails a high step-up dc-dc converter.

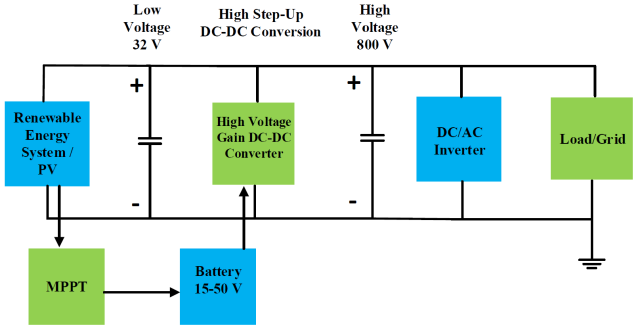

FIGURE 1. High step-up dc-dc converter for a PV system.

High step-up dc-dc converters with high efficiency have been proposed in [3]. These converters have utilized active clamps to recycle the leakage energy and mitigate the output diode reverse recovery issue. Diminishing the resonance between the leakage inductance and the capacitance of the devices plays a vital role in alleviating the voltage stresses. In 2013, a novel high step-up dc-dc converter for distributed generation systems has been introduced, and the voltage conversion ratio has been increased due to utilizing a coupled inductor and two capacitors [4]. The proposed converter in [5] has achieved a very high step-up voltage gain by integrating two coupled inductors and switched capacitor techniques. Moreover, the conduction losses have been alleviated due to the low resistance, which would result in increasing the efficiency and reducing the reverse recovery of the diodes. In [6], high efficiency with high step-up dc-dc converter and dual coupled inductors for grid-connected photovoltaic systems has been presented. In addition, this proposed converter has used an integrated regenerative snubber to recycle the leakage energy to the output and has also employed active clamp circuits with a shared clamp capacitor on the active switches. The proposed converters in [7] and [8] have offered a high step-up dc-dc converter by using coupled inductor and voltage-lift technique. In addition, the voltage stress has been reduced, and the conversion efficiency has been improved. In [9], a high step-up voltage gain active-network converter with switched-capacitor but without using a high duty cycle has been provided, and the low voltage components can be utilized to reduce the conduction loss and cost. A cascade cockcroft–walton voltage multiplier has been applied to a transformerless high step-up dc-dc converter, and then the proposed control strategy comprises two different frequencies, one of which has operated at high frequency to mitigate the size of the inductor, and the other one operates at a low frequency to reduce the output voltage ripple [10]. The conventional boost converter theoretically can achieve a high output voltage by using a very large duty cycle. However, operating at the extreme high duty cycles would result in high conduction losses and would make the semiconductors suffer the voltage stress [11]. In [12], a high step up quasi z-source dc-dc converter with coupled inductors has been presented, and the main benefits of the aforementioned converter are low normalized voltage stress on semiconductors compared to the quasi z-source and continous input current. Furthermore, the conventional boost converter experiences a low efficiency due to the instability, power dissipation and complexity of the control part. Cascaded boost converter could be used to increase the output voltage since it consists of two conventional boost converters without using extreme duty cycles. However, using cascaded boost converter would increase the components size and result in high ripples on the input current, and the output diode may experience extreme voltage stress on the switches. In addition, the energy will be processed twice and that would eventually compromise the efficiency. A switched capacitor dual switch high step-up dc–dc is introduced, the waveforms have been explored in the continuous conduction mode and the discontinuous mode, and the conduction losses have been reduced due to the small duty cycle [13]. The aforementioned proposed topologies may suffer from diode reverse recovery and electromagnetic interference problems.

On the other hand, using isolated dc-dc converters is another voltage boost technique to lift the voltage gain which would utilize the coupled inductors and transformers [14]–[19]. Employing high frequency transformers can boost the input voltage and offer the electrical isolation to protect the circuit [20]–[24]. But using a transformer can cause the leakage inductance and reduce the power density [25]–[28]. Coupled inductors have the flexibility compared to transformers to boost the output voltage [29]–[32]. Consequently, achieving a high voltage gain requires an increase in the turns ratio, which may cause the leakage inductance and the voltage spikes in isolated dc-dc converter. Zero current-switching (ZCS) turn-ON soft-switching performance for the switches is utilized, which would reduce the electromagnetic interference (EMI) noises and the switching losses. This paper presents the operational principle of the proposed converter in section II, modes of operation in part A of section II, voltage gain analysis and performance comparison in part B of section II, design consideration and simulation results in

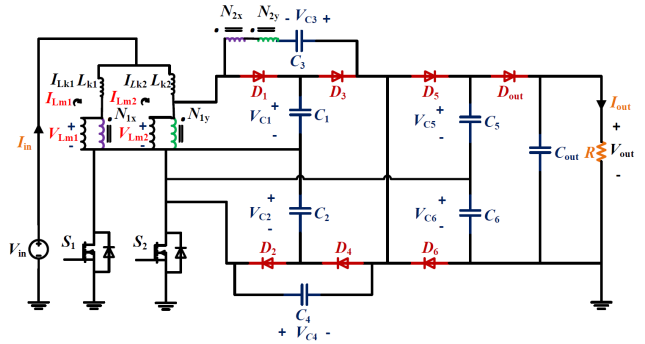

FIGURE 2. The proposed high step-up dc-dc converter.

section III, voltage and current stress on the switches in part A of section III, inductor design in part B of section III, voltage and current stress on the diodes in part C of section III, voltage and current stress on the capacitors in part D of section III, efficiency analysis in part E of section III, experimental results in section IV, and conclusion in section V.

II. OPERATIONAL PRINCIPLE OF THE PROPOSED CONVERTER

The proposed converter primarily consists of two parts; the first part is the interleaved boost converter with coupled inductors, and the second part is the voltage multiplier cells and the secondary windings, which can extend the voltage gain and mitigate the current ripple. A high step-up interleaved boost converter with coupled inductors and voltage multiplier is shown in Fig. 2. The interleaved boost converter has two coupled inductors, the magnetizing inductors L_{m1} and L_{m2}, the leakage inductances L_{k1} and L_{k2} and two switches connected to a single source. The secondary windings of the coupled inductors are connected with the voltage multiplier. Voltage multiplier cells have some diodes and capacitors, and they are connected to the load to overcome the voltage discrepancy that may occur. The proposed converter works only in the continuous conduction mode (CCM)since the inductor current does not reach zero and based on that, the operational principle and the steady state analysis are in CCM. The diode reverse recovery can be mitigated by the leakage inductance of the coupled inductors. The proposed converter shares the primary side of the coupled inductors and integrates them to the secondary side. By increasing the phases of the interleaved converter, the ripple on the input current will decrease. Fig. 3 shows the switching signals of the proposed converter, and the phase shift between the switches is 180 degree. In addition, there are some assumptions in order to simplify the circuit; the semiconductor devices are ideal, both inductor currents are operated in the conduction continuous mode, the coupled inductors are modeled ideally with a magnetizing inductor and a leakage inductor and an ideal transformer with a turns ratio of

$$N = \frac{N_{1y}}{N_{1x}} = \frac{N_{2y}}{N_{2x}} \tag{1}$$

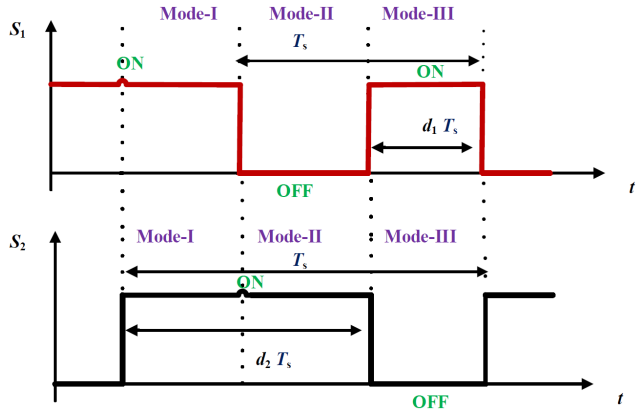

FIGURE 3. The Switching signals of the proposed converter.

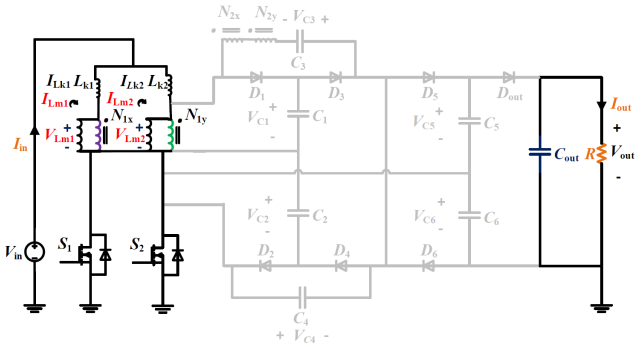

FIGURE 4. Mode-I of operation for the proposed converter.

A. MODES OF OPERATION

The operation modes and the typical performance of the proposed converter are presented in the continuous conduction mode (CCM).

Mode-I: S_1 and S_2 are ON and, they are conducting in the mode as shown in Fig. 4. L_{m1} and L_{m2} store the energy. Moreover, the magnetizing inductors L_{m1} and L_{m2}, the leakage inductances L_{k1} and L_{k2} are charged by the dc input voltage. The magnetizing inductor currents are linearly increased. It can be observed that the diodes of voltage multiplier cells do not conduct, and they are reverse biased. In addition, the output diode D_{out} is reverse biased, and the capacitor voltages of the voltage multiplier cells remain fixed. Finally, the load energy is supplied by the output capacitor C_{out}.

Mode-II: In this mode, S_1 is OFF and S_2 is ON as shown in Fig. 5. D_1, D_4 and D_5 do not conduct, then they are reverse biased. L_{m2} stores the energy, and L_{m1} release the energy. However, D_2, D_3, D_6 and the output diode D_{out} are forward biased and conduct in this state. The magnetizing inductance L_{m1}, the leakage inductance L_{k1} and the source charge C_2, C_3 and C_6. On the other hand, L_{m2} and L_{k2} are charged by the dc input voltage.

Mode-III: S_1 is ON and S_2 is OFF as shown in Fig. 6. D_2, D_3, D_6 and the output diode D_{out} are reverse biased, and they are OFF. But D_1, D_4 and D_5 are conducting, and they are forward biased. L_{m2} and the input voltage charge C_1, C_4 and

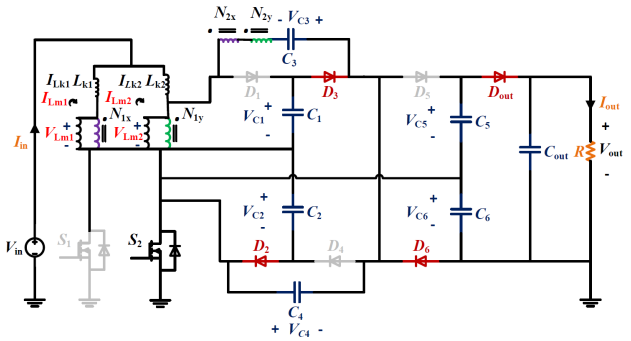

FIGURE 5. Mode-II of operation for the proposed converter.

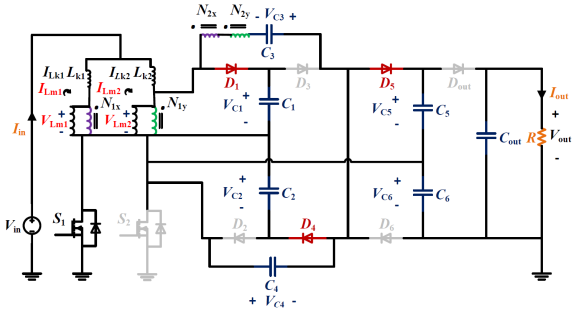

FIGURE 6. Mode-III of operation for the proposed converter.

C_5. L_{m1} stores the energy, and the magnetizing inductance L_{m2}, and the leakage inductance L_{k2} transfers the energy.

B. VOLTAGE GAIN ANALYSIS AND PERFORMANCE COMPARISON

The mathematical expression of the voltage gain is calculated in this part. For the second mode, the steady state equations can be expressed as

$$\langle V_{\mathrm{Lm1}} \rangle = 0 \tag{2}$$

$$V_{\mathrm{in}} = \frac{dI_{\mathrm{Lm1}}}{dt} \tag{3}$$

$$V_{\mathrm{in}} = \frac{dI_{\mathrm{Lm2}}}{dt} \tag{4}$$

$$\int_0^{DT_s} V_{\mathrm{Lm1}} dt + \int_{DT_s}^{T_s} V_{\mathrm{Lm2}} dt = 0 \tag{5}$$

The capacitor voltages for C_1 and C_2 are equal, the magnetizing voltages are identical and can be derived as

$$V_{\mathrm{Lm1}} = V_{\mathrm{Lm2}} = V_{\mathrm{in}} + V_{\mathrm{C1}} - V_{\mathrm{C2}} \tag{6}$$

$$V_{\mathrm{Lm1}} = V_{\mathrm{Lm2}} = V_{\mathrm{in}} \tag{7}$$

For mode-III, the capacitor voltages for C_1 and C_2 can be given as

$$V_{\mathrm{C1}} = V_{\mathrm{C2}} = V_{\mathrm{in}} \times \frac{1}{(1-D)} \tag{8}$$

The capacitor voltages for C_5 and C_6 are twice the capacitor voltages for C_1 and C_2. By applying the volt-second balance principle, the ideal voltage gain can be written as, the number of turns ratio is 3 and can be computed as

$$M = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = 2(N+1) \times \frac{1}{(1-D)} = 8 \times \frac{1}{(1-D)} \tag{9}$$

The voltage gain conversion can be written as

$$V_{\mathrm{out}} = V_{\mathrm{in}} \times \frac{8}{(1-D)} \tag{10}$$

The performance comparison between the proposed converter and other topologies is shown in TABLE 1. The main characteristics include voltage gain, voltage stresses on switches and diodes, total number of components, such as switches, diodes, capacitors and inductors, sharing ground connection and the input current. It can be noted from TABLE 1 that the voltage stresses and the voltage gain of the proposed converter are equal to [6]. In addition, the voltage stress across switches and diodes in [10] are identical to the voltage stress across switches for the proposed converter. However, even though the voltage stress across devices in [10] are identical and reduced, the number of switches is four, which results in increasing the cost and the size of the converter. The converter in [15] suffers from the high voltage stress across switches and diodes, and the stresses across semiconductors are equal to the output voltage, and as a result, the performance of the converter becomes very low, and the input current is discontinuous. The duty cycle in [9] is low, the voltage stresses across power devices are alleviated, the number of components is small, and then the reliability of this converter is high. However, the voltage gain for the converter is low compared to the proposed converter. The topology in [11] has a high voltage stress on diodes compared to the proposed converter, and it is identical to the output voltage. Thus, this converter is not suggested for high step-up applications. Converters in [12], [13] and [14] have a very small duty cycle, which leads to decreasing the power losses, but in [13] the voltage gain ratio is small compared to the proposed converter.

Fig. 7 illustrates that the relationship between the voltage gain (M) and the duty cycle (D) with several turns ration, and it can be observed that as the turns ratio (N) increases, the voltage gain proportionally increases. In addition, the proposed converter offers a high voltage gain without an extreme high duty cycle. The derivation of the turns ration formula will be discussed in part B of section III.

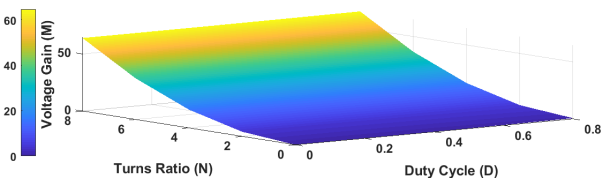

FIGURE 7. Voltage gain (M) vs. duty cycle (D) of the proposed converter with several turns ratio (N).

TABLE 1. Performance comparison between the proposed converter and other topologies.

Topologies	Voltage gain (M) $(V_{\text{out}}/V_{\text{in}})$	Voltage stress on switches	Voltage stress of diodes	No. of components			No. of inductor cores		Shared grounded	Input Current
				S	D	C	Single	Coupled		
Ref. [5]	$\frac{2N+4}{1-D}$	$\frac{1}{2N+4}$	$\frac{N+1}{N+2}$	2	4	4	0	2	Yes	Continuous
Ref. [6]	$\frac{2(N+1)}{1-D}$	$\frac{V_{\text{out}}}{2(N+1)}$	$\frac{(2N+1)V_{\text{out}}}{2(N+1)}$	4	2	3	0	2	Yes	Continuous
Ref. [9]	$\frac{3+D}{1-D}$	$\frac{V_{\text{out}}}{2}$	$\frac{V_{\text{out}}}{2}$	1	1	1	0	2	No	Discontinuous
Ref. [10]	$\frac{2N}{1-D}$	$\frac{V_{\text{in}}}{(1-D)}$	$\frac{2V_{\text{in}}}{(1-D)}$	4	6	6	1	0	No	Continuous
Ref. [11]	$\frac{2(N+1)}{1-D}$	$\frac{V_{\text{out}}}{2(N+1)}$	V_{out}	4	4	5	2	1	Yes	Continuous
Ref. [12]	$\frac{2+N}{1-D}$	$\frac{V_{\text{in}}}{(1-2D)}$	$\frac{(1+N)V_{\text{in}}}{1-2D}$	1	4	5	1	1	No	Continuous
Ref. [13]	$\frac{3-2D}{1-2D}$	$\frac{V_{\text{out}}-V_{\text{in}}}{2}$	$\frac{V_{\text{out}}-V_{\text{in}}}{2}$	2	4	3	1	0	No	Continuous
Ref. [14]	$\frac{(1+ND)}{1-D}$	$\frac{V_{\text{out}}}{(1+ND)}$	$\frac{(1-D)NV_{\text{out}}}{(1+ND)V_{\text{in}}}$	1	2	3	2	1	No	Continuous
Ref. [15]	$\frac{1}{1-2D}$	V_o	V_{out}	1	2	3	2	0	Yes	Discontinuous
Ref. [16]	$\frac{2(N+1)}{1-D}$	$\frac{V_{\text{in}}}{1-D}$	$\frac{2NV_{\text{in}}}{1-D}$	2	4	3	0	2	Yes	Continuous
Ref. [26]	$\frac{2(N+1)}{1-D}$	$\frac{V_{\text{out}}}{2(N+1)}$	$\frac{NV_{\text{out}}}{N+1}$	2	4	4	0	2	Yes	Continuous
Proposed converter	$\frac{2(N+1)}{1-D}$	$\frac{V_{\text{in}}}{1-D}$	$\frac{2V_{\text{in}}}{1-D}$	2	7	7	0	2	No	Continuous

III. DESIGN CONSIDERATIONS AND SIMULATION RESULTS

A. VOLTAGE STRESS ON THE SWITCHES

The voltage stress on the switches is significantly reduced to 100 V, the input current is 24.25 A, and the output current is 0.97 A as depicted in Fig. 8. The voltage stress on the switches can be derived as

$$V_{\text{sw1}} = V_{\text{sw2}} = V_{\text{in}} \times \frac{1}{(1-D)} \tag{11}$$

The peak current stress across the active switches can be expresses as

$$I_{\text{sw1(peak)}} = I_{\text{sw2(peak)}} = \frac{2(N+1)I_{\text{out}}}{(1-D)} \tag{12}$$

The average current stress on the active switches can be given as

$$I_{\text{sw1(avg)}} = I_{\text{sw2(avg)}} = \frac{(N+1)I_{\text{out}}}{(1-D)} \tag{13}$$

The benefit of having MOSFETs switches is that MOSFETs can magnificently run at high frequencies. The average current stress across the active switches is 12.125 A. Since the voltage stress across switches is reduced, the low on-state resistance MOSFETs can be used to improve the efficiency.

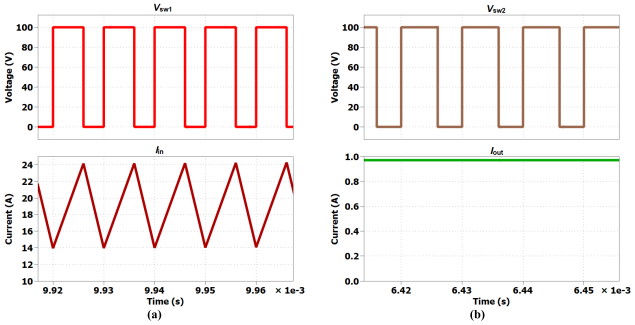

FIGURE 8. The voltage stress on the active switches, the input current and the output current.

B. INDUCTOR DESIGN

The turns ratios of the coupled inductors play a significant role in determining the voltage and current stress across the power devices. The average magnetizing inductor currents rely on the turns ratio (N). It can be observed that the magnetizing inductor currents of the coupled inductors are balanced because of the charge balance of the capacitors. The average magnetizing inductor currents can be calculated as

$$I_{\text{Lm(avg)}} = I_{\text{Lm1(avg)}} = I_{\text{Lm2(avg)}} = \frac{(N+1)I_{\text{out}}}{(1-D)} \tag{14}$$

The average input current is twice the average magnetizing inductor currents and can be written as

$$I_{\text{in}} = 2 \times I_{\text{Lm1(avg)}} = 2 \times I_{\text{Lm2(avg)}} \tag{15}$$

$$I_{\text{in}} = \frac{2(N+1)I_{\text{out}}}{(1-D)} \tag{16}$$

For the second mode, the second leakage inductor current

$$I_{\text{Lk2}} = I_{\text{Lm1(avg)}} + I_{\text{Lm2(avg)}} \tag{17}$$

For the third mode, the first leakage inductor current

$$I_{\text{Lk1}} = I_{\text{Lm1(avg)}} + I_{\text{Lm2(avg)}} \tag{18}$$

The magnetizing current ripple can be given as

$$\Delta I_{\text{Lm}} = 0.15 \times I_{\text{Lm(avg)}} \tag{19}$$

The magnetizing inductances are designed based on the input current and can be calculated as

$$L_{\text{m1}} = L_{\text{m2}} = \frac{DV_{\text{in}}}{f_{\text{sw}} \Delta I_{\text{Lm}}} \tag{20}$$

Determining the turns ratio plays a significant role in obtaining the voltage gain, voltage stress on the switches and voltage stress on the diodes. Therefore, since the duty cycle is 0.68, the output voltage is 800 V, and the input voltage is 32 V. The duty cycle D during the steady state is larger than 0.5. The magnetizing voltages and the average magnetizing inductor currents are illustrated in Fig. 9. Each magnetizing voltage is 32 V, and each average magnetizing inductor currents is 12.125 A.

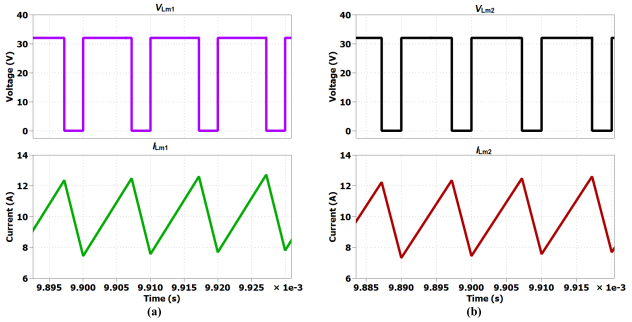

FIGURE 9. The magnetizing voltages and the average magnetizing inductor currents.

C. VOLTAGE AND CURRENT STRESS ON THE DIODES

The voltage stress across diodes is twice the voltage stress on active switches. The maximum voltage stress across the diodes can be expressed as

$$V_{\text{D(max)}} = V_{\text{in}} \times \frac{2}{(1-D)} \tag{21}$$

The average currents stress on the diodes can be derived as

$$I_{\text{D(avg)}} = I_{\text{out}} = \frac{V_{\text{out}}}{R} \tag{22}$$

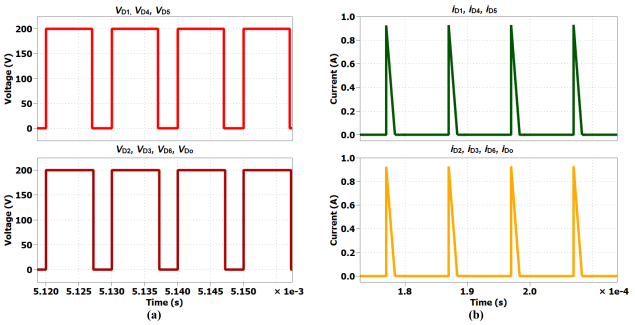

FIGURE 10. The voltage and current stresses on the diodes.

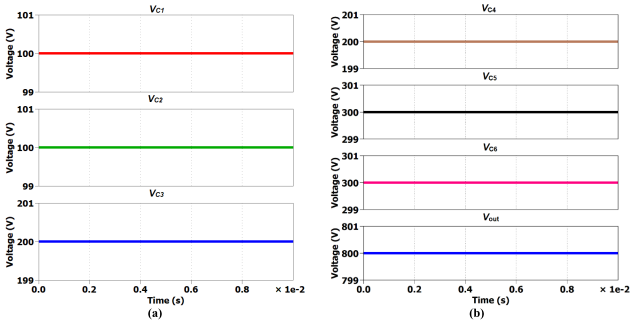

FIGURE 11. The voltage stress on capacitors.

The voltage stress across diodes is alleviated to 200 V, and the average currents stress on the diodes is 0.97 A as shown in Fig. 10. It can be noted that the voltage stress across diodes increases when the turns ratio increases. However, it is lower than the output voltage.

D. VOLTAGE STRESS ON THE CAPACITORS AND CAPACITOR DESIGN

The current stress across capacitors can be written as

$$I_{\text{C(rms)}} = I_{\text{out}} \tag{23}$$

It can be seen that due to the leakage inductances, the reverse recovery problems of the diodes are mitigated. The voltage stress on C_1 is 100 V, on C_2 is 100 V, C_3 is 200 V and on C_4 is 200 V, C_5 is 300 V, C_6 is 300 V, and the output voltage is boosted to 800 V as illustrated above in Fig. 11.

The capacitor design is controlled by the voltage ripple of the capacitors, x is the number of any desired capacitors, and then the output voltage ripple, and the capacitor design can be derived as

$$\Delta V_{\text{out}} = \frac{(1-D)I_{\text{out(rms)}}}{C_{\text{x}} f_{\text{sw}}} \tag{24}$$

$$C_{\text{x}} = \frac{(1-D)I_{\text{c(rms)}}}{\Delta V_{\text{cx}} f_{\text{sw}}} \tag{25}$$

E. EFFICIENCY ANALYSIS

When both switches S_1 and S_2 conduct at the same, power loss would occur. There are two power losses; conduction

TABLE 2. Simulation of component parameters.

Parameter	Value
Input voltage	32 V
Output voltage	800 V
Duty Cycle	0.68
Load resistance	825 Ω
Magnetizing Inductors	94 µH
Frequency (f_{sw})	118 kHz
Capacitors	10 µF

losses and switching losses. The conduction losses are caused by the parasitic resistance of the components. In addition, the conduction loss in switches is caused by the resistance of MOSFETs during conduction time and can be given as

$$P_{\text{sw(con loss)}} = (I_{\text{sw(rms)}} \times I_{\text{sw(rms)}})R_{\text{DS(on)}} \tag{26}$$

where $R_{\text{DS(on)}}$ is the drain source when the switch is ON, the switching loss in the switches can be derived as

$$P_{\text{sw(loss)}} = \frac{V_{\text{sw1}} I_{\text{sw}} (T_{\text{on,sw1}} + T_{\text{off,s1}}) f_{\text{sw}}}{2} + \frac{V_{\text{sw2}} I_{\text{sw}} (T_{\text{on,sw2}} + T_{\text{off,s2}}) f_{\text{sw}}}{2} \tag{27}$$

The losses in diodes are equal to 2.91 W and include the forward voltage, and the average diode currents, which are identical to the output current and can be expressed as

$$P_{\text{D(loss)}} = I_{\text{D(avg)}} \times V_{\text{F}} \tag{28}$$

where V_{F} is the forward voltage of the diodes. The power losses in capacitors are caused by the equivalent series resistance of the capacitor and can be derived as

$$P_{\text{C(loss)}} = (I_{\text{C(rms)}} \times I_{\text{C(rms)}}) \times \text{ESR} \tag{29}$$

The conduction loss of the coupled inductors in the DC resistance can be calculated as

$$P_{\text{L(Cond loss)}} = (I_{\text{L(rms)}} \times I_{\text{L(rms)}}) \times R_{\text{L(DC)}} \tag{30}$$

The core losses of the coupled inductors can be explored by using Steinmetz coefficients.

$$P_{\text{Core(loss)}} = K \times f^{\alpha} \times B_{\text{max}}^{\beta} \times I_{\text{c}} \times A_{\text{c}} \tag{31}$$

The total power loss of the proposed converter can be written as

$$P_{\text{loss(total)}} = P_{\text{SW(cond)}} + P_{\text{SW}} + P_{\text{D}} + P_{\text{C}} + P_{\text{L}} + P_{\text{Core(loss)}} \tag{32}$$

Consequently, the efficiency of the proposed converter can be calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss(total)}}} \tag{33}$$

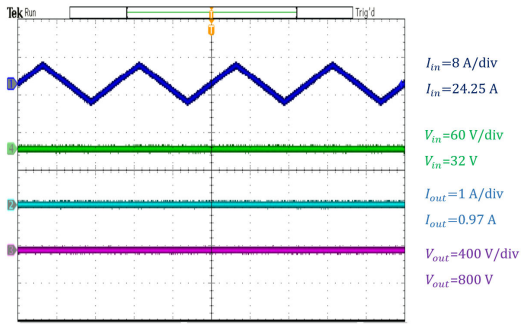

FIGURE 12. The input current, the input voltage, the output current and the output voltage.

TABLE 3. List of components for the experimental parameters.

Components	Description
MOSFETs (S_1, S_2)	IAUT300N08S5N014 ($R_{\text{ds(on)}} = 1.4\text{m}\Omega, 80\text{ V}, 300\text{ A}$)
Diodes ($D_1 - D_{\text{out}}$)	DPG20C300PN (300 V, 10 A, 35 ns)
Capacitors ($C_1 - C_{\text{out}}$)	C4ATMBW5100A3NJ (10 µF, 850 V)
Coupled Inductor (L_{m})	EDT31 ferrite core, B66397 (94 µH, N87 material)

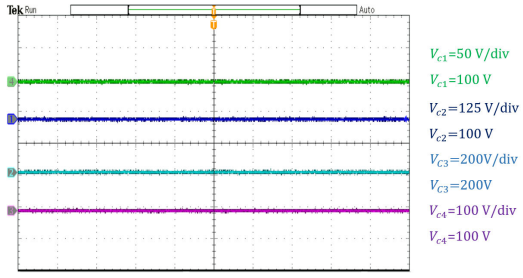

FIGURE 13. The voltage stress on the capacitors.

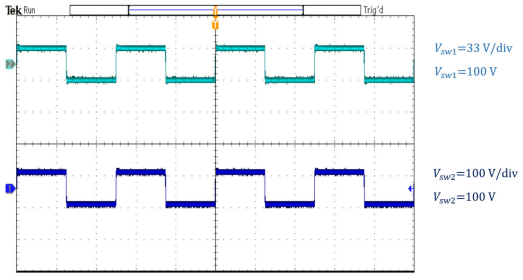

FIGURE 14. The voltage stress on the switches.

IV. EXPERIMENTAL RESULTS

A hardware prototype has been built to validate the design and the simulation results. TABLE 3 shows the components and the description of the experimental results.

The switching frequency is selected to be 118 kHz, and the load resistance is chosen to be 825 Ω. The components used to implement the prototype are shown in TABLE 1. The converter is rated at 400 W with input voltage of 32 V and

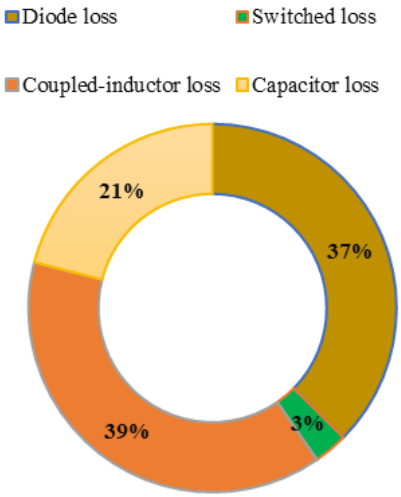

FIGURE 15. The power loss breakdown.

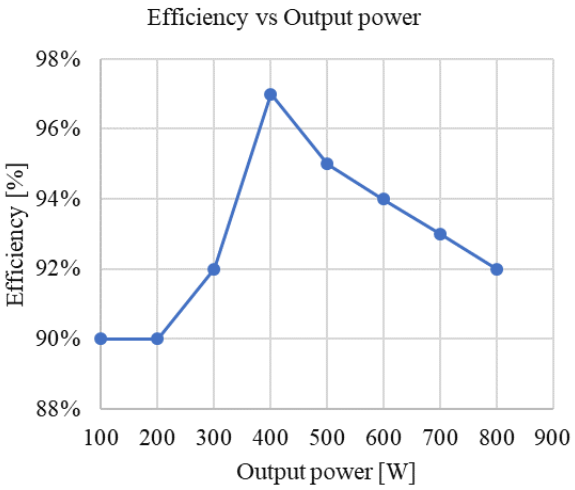

FIGURE 16. The output power (P_{out}) and the efficiency.

output voltage of 800 V. The active switches are performed by using MOSFETs IAUT300N08S5N014 for their low $R_{ds(on)}$ and low switching power loss. The high performance and fast recovery DPG20C300PN diodes are selected to achieve the voltage blocking on diodes. The capacitors are accomplished by using film capacitors C4ATMBW5100A3NJ to implement the voltage blocking and the output capacitor on the load. The magnetizing inductor is attained using coupled inductor and magnetic core of EDT31 ferrite core, B66397 and N87 material.

The input current is 24.25 A, the input voltage is 32 V, the output current is 0.97 A and the output voltage is 800 V as shown in Fig. 12. The voltage stress on capacitors is depicted in Fig. 13. Fig. 14 shows the voltage stresses on the active switches, which are reduced to 100 V.

The power loss breakdown of the proposed converter is illustrated in Fig. 15, and it can be observed that the dominant power losses are the coupled inductor loss, the diode loss, the capacitor loss and the switch loss. To enhance the efficiency of the proposed converter, more coppers are highly recommended. Fig. 16 illustrates the output power (P_{out})and the efficiency (η) of the proposed converter.

The peak efficiency of the proposed converter is 96.7% at the output power of 400 W in diverse loads. In addition, it can be noted that the maximum efficiency occurs at 400 W.

V. CONCLUSION

An interleaved high step-up dc–dc converter with coupled inductors and voltage multiplier has been proposed for renewable energy applications. The proposed converter has been successfully designed to achieve a very high step-up voltage gain without an extreme duty cycle or a high turns ratio. The aforementioned converter was considerably implemented to lift a 32 V to 800 V. The structure of the proposed converter could be extended for a higher step-up voltage gain, and the turns ratio could be increased for further voltage gain. The voltage stress across semiconductors was considerably decreased. The input current ripple was remarkably reduced due to the interleaved structure in the primary side. The reverse recovery problem of the diodes was alleviated, and the leakage energy was recycled. The MOSFETs with a small ON-resistance and low-voltage-rated were utilized to mitigate the conduction losses and the voltage stress on the switches. The analysis of the operational principle for the proposed converter was implemented, and the comparison between the suggested converter and other topologies was introduced. Moreover, the design consideration, simulation results and the experimental verifications were presented thoroughly. A 400 W hardware prototype was tested to verify the theoretical analysis and the design. The maximum efficiency was measured to be 96.7%. Therefore, the proposed converter was greatly suitable for interfacing renewable energy applications, which required high voltage gain and high efficiency.

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